REMARKS

Rejection Under 35 U.S.C. § 103(a)

In paragraph 3 of the Office Action, the Examiner asserts that, "Claims 1, 2, 5-8, 10, 11, 14-16, & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio et al.,(U.S. Patent number 5867642) in view of Hasbiguchi et al., (U.S. Patent number 5261084).

Amended independent claim 1 now claims:

"identifying a predetermined instruction sequence containing a memory access request;

checkpointing a predetermined set of system data;

executing the memory access request after the checkpointing;

monitoring for memory access errors;

logging any memory access errors in an error logging register;

polling the register for any logged memory access error during execution of the instruction sequence;

raising exceptions, if any memory access error is logged; and

recovering from any memory access error using the checkpointed system data, if the memory access error is logged during execution of the instruction sequence."

Antecedent basis for this amendment is found in Figure 3, steps 302 through 318 of the specification. According to the elements of claim 1, checkpointing of system data

is performed *before* executing the memory access request, and the checkpointed system data is used to recover from *any* memory access error logged during execution of the instruction sequence.

Neither Vivio nor Hasbiguchi alone or in view of each other teaches or suggests performing checkpointing before execution, nor using such checkpointed data to recover from *any* memory access error. Vivio even teaches away from the present invention.

More specifically, Vivio at col. 7, lns. 44-56 states that "An area of memory is reserved and an acceptable error frequency level is determined, ... For each memory access, the accessed memory area is checked for an error, ... If an error is found, it is logged for the memory area from which it occurred, ... The error log for each memory area is compared to the error frequency level ... . If the level is not exceeded, normal operation continues. If the level is exceeded, concurrent writes are enabled 360, and the memory area which exceeded the level is copied 370 in small blocks to the reserve memory area. When copying is completed, accesses are remapped to the reserve memory area 380, and normal operation is resumed." Thus, Vivio teaches "concurrent writes" and copying "the memory area which exceeded the level" only *after* determining that an "error frequency level" has been exceeded (i.e. *after* executing a memory access request). In contrast, the present invention claims checkpointing system data *before* executing a memory access request.

Furthermore, unlike the present invention, Vivio only begins such copying and "concurrent writes" if an "error frequency level" has been exceeded. In contrast, the present invention claims "recovering from any memory access error" and not just if multiple errors have occurred (i.e. an error frequency has been exceeded).

Similarly, Hasbiguchi neither teaches nor suggests alone or in view of Vivio the claimed invention's checkpointing of system data *before* executing the memory access request, or using the checkpointed system data to recover from *any* memory access error logged during execution of the instruction sequence. Therefore, Applicants assert that amended independent claim 1 is now in condition for allowance.

Claims 3-8 depend from claim 1 and the Applicants respectfully submit that they are allowable for at least the same reasons. Furthermore, claim 5 recites "masking a machine check abort handle" which is neither taught nor suggested by Vivio at (col. 2, lines 57-59). Vivio's statement that his "invention avoids errors for devices and applications that can not tolerate long delays in accessing memory" is a conclusion and not a specific teaching of "how" Vivio would effect such error avoidance. In contrast, the Applicants' claimed machine check abort handle masking is a very specific and clear action. In fact, nowhere in Vivio is use of a machine check abort handle for "error avoidance" discussed. Similarly, claim 6 recites "enabling the machine check abort handle" which is also neither taught nor suggested by Vivio at (col. 2, lines 57-59), nor anywhere else in Vivio.

Independent claims 10 and 15 have been amended in a manner equivalent to claim 1 and Applicants respectfully submit that they are allowable for at least the same reasons. Also, claims 11-14 and 16-19 respectively depend from claims 10 and 15 and Applicants respectfully submit that they are also allowable for at least the same reasons as discussed with respect to claims 3-8.

Allowable Claim

In paragraph 6 of the Office Action, the Examiner states that "Claim 9 is allowed." In response Applicants retain claim 9 as originally filed.

Objection to the Claims

In paragraph 7 of the Office Action, the Examiner states that "Claims 3, 4, 12, 13, 17 & 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

In response, Applicants have add new claims 20-25 which claim the subject matter within claims 3, 4, 12, 13, 17 & 18 respectively and include all the limitations of their base claims as well as the limitations of any intervening claims. Thus, claims 20-25 are in condition for allowance.

Reconsideration and allowance of claims 1-19 and of new claims 20-25 is respectfully requested. The Applicants respectfully submit that no new matter has been introduced by these amendments or additions to the claims.

Should the Examiner find any remaining impediment to allowance of these claims that could be resolved by a telephone conference, please call the undersigned.

Respectfully submitted,
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